

## **REMARKS**

Claims 21-37 are pending in this application. Claims 1-20 have been canceled without prejudice or disclaimer. The Examiner rejected Claims 21-37 under either 35 U.S.C. § 102(e) or 35 U.S.C. § 103 as allegedly being either anticipated or obvious in view of the cited references. The Applicants traverse the rejections as follows.

### **Anticipation Rejections**

The Examiner rejected Claims 21-26 and 28-37 under 35 U.S.C. § 102(e) as allegedly being anticipated by one of three references: (1) United States Patent Application Publication No. 2003/0233494 to Ghosh *et al.* (the “Ghosh publication”), (2) United States Patent Application Publication No. 2004/0148376 to Rangan *et al.* (the “Rangan publication”), or (3) United States Patent

Application Publication No. 2004/0010612 to Pandya *et al.* (the “Pandya publication”). The Applicants traverse the rejections because none of the cited references teaches every limitation of the claims.

With respect to Claim 21, none of the cited references teaches every one of the following limitations:

- “a storage network processor (SNP) configured to offload at least some packet processing tasks from a general purpose processor associated with a host device, the storage network processor further comprising:”
  - “a hardware-accelerated receive module configured to receive TCP network packets;”
  - “a hardware-accelerated TCP and iSCSI protocol processing chip configured to process both TCP network packets and iSCSI instructions embedded in TCP network packets, wherein processing of iSCSI instructions embedded in TCP network packets includes offloading common case iSCSI instructions embedded in TCP network packets to process and resolve the embedded iSCSI instructions in hardware; and”
  - “a hardware-accelerated transmit module configured to transmit TCP network packets.”

For example, none of the references teaches a processing chip that processes “both TCP network packets and iSCSI instructions embedded in TCP network packets” in the manner recited by Claim 21. Accordingly, Claim 21 is patentable over the cited references at least based on the distinctions set forth above.

Dependent Claims 22-37 incorporate all of the limitations of Claim 21 and are thus patentable for the same reasons that Claim 21 is patentable. Moreover, Claims 22-37 are also patentable based on their additional limitations. Accordingly, the Applicants respectfully request that the Examiner withdraw the anticipation rejections.

#### **Obviousness Rejections of Claim 27**

The Examiner rejected Claim 27 as allegedly being obvious in view of either the Ghosh publication, the Rangan publication, or the Pandya publication and the Examiner’s official notice that, allegedly, “both the concept and advantages of providing the line rate is approximately 10 Gigabit/sec is well known and expected in the art.”

The Applicants respectfully traverse the Examiner’s taking of official notice. The cited references do not show that the disclosed systems can achieve a line rate of 10 Gigabits per second. Indeed, the Pandya publication makes it clear that certain implementations (such as software TCP/IP implementations) may be unable to achieve line rates above 1 Gbps. See Pandya ¶ 0094. Thus, the line rate that a system can achieve depends on the system’s architecture, and it cannot merely be assumed without evidence that any particular system can achieve a line rate of 10 Gigabits per second. As the Applicants have traversed the taking of official notice, the Examiner “must provide documentary evidence in the next Office action if the rejection is to be maintained.” M.P.E.P. § 2144.03(C).

For the foregoing reasons, the Applicants request that the Examiner withdraw the taking of official notice and withdraw the obviousness rejections of Claim 27.

#### **Note about the Drawings**

The Applicants note that page 2 of the Office Action states that “[t]he figures submitted on 7/19/2004 are acknowledged,” but that the Office Action Summary indicates that “[t]he drawing(s) filed on 17 February 2004 is/are: . . . objected to by the Examiner.” Accordingly, the Applicants’ attorney sought clarification from the Examiner about whether there is any objection to the drawings.

**Application No.:** 10/781,338  
**Filing Date:** February 17, 2004

**No Disclaimers or Disavowals**

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. The Applicants reserve the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that the Applicants have made any disclaimers or disavowals of any subject matter supported by the present application.

**Co-Pending Applications of Assignee**

Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee.

<b>Serial Number</b>	<b>Title</b>	<b>Filed</b>
10/781,341	REMOTE DIRECT MEMORY ACCESS FOR ISCSI	February 18, 2004
11/835,942	STORAGE CONTROLLER REDUNDANCY USING PACKET-BASED PROTOCOL TO TRANSMIT BUFFER DATA OVER REFLECTIVE MEMORY CHANNEL	August 8, 2007
10/781,552	NETWORK RECEIVE INTERFACE FOR HIGH BANDWIDTH HARDWARE-ACCELERATED PACKET PROCESSING	February 17, 2004
12/140,101	SYSTEM AND METHODS FOR HIGH RATE HARDWARE-ACCELERATED NETWORK PROTOCOL PROCESSING	June 16, 2008

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Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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